



VHDL for Engineers

By Kenneth L. Short

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Suitable for use in a one- or two-semester course for computer and electrical engineering majors.

VHDL for Engineers, First Edition is perfect for anyone with a basic understanding of logic design and a minimal background in programming who desires to learn how to design digital systems using VHDL. No prior experience with VHDL is required. This text teaches readers how to design and simulate digital systems using the hardware description language, VHDL. These systems are designed for implementation using programmable logic devices (PLDs) such as complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs). The book focuses on writing VHDL design descriptions and VHDL testbenches. The steps in VHDL/PLD design methodology are also a key focus. Short presents the complex VHDL language in a logical manner, introducing concepts in an order that allows the readers to begin producing synthesizable designs as soon as possible.

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Editorial Review

From the Back Cover

This book teaches readers how to design and simulate digital systems using the hardware description language, VHDL. Focus is placed on writing VHDL design descriptions, VHDL testbenches, and the steps in VHDL/PLD (programmable logic devices) design methodology. Topics include: Digital Design using VHDL and PLDs; Entities, Architectures, and Coding Styles; Signals and Data Types; Dataflow and Behavioral Style Combinational Design; Event-Driven Simulation; Testbenches for Combinational Designs; Latches and Flip-Flops; Multibit Latches, Registers, Counters, and Memory; Finite State Machines; ASM Charts and RTL Design; Subprograms; Packages; Testbenches for Sequential Systems; Modular Design and Hierarchy. More than 275 block diagrams, logic diagrams, and timing waveforms and 180+ program listings illustrate the design concepts. The book includes the Aldec Active-HDL(tm) 7.2 Student Edition Software.

This book is suitable for anyone with a basic understanding of logic design and a minimal background in programming who desires to learn how to design digital systems using VHDL. No prior experience with VHDL is required.

About the Author

Short of the State University of New York at Stony Brook.

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